ABSTRACT

A cache coordination mechanism for a multiprocessor, shared-memory computer switches between a snooping mechanism where an individual processor unit broadcasts or multicasts cache coherence messages to each other node on the system and a directory system where the individual processor unit transmits the cache control message to a directory which then identifies potential candidates to receive that message. The switching is according to the activity on the communication network used by the cache coherence messages. When network activity is high, a directory protocol is used to conserve bandwidth but when network activity is low, a snooping system is used to provide faster response.

MKE/5129931